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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,996	09/24/2003	Pascal Janin	02GR220254483	4508

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,996	JANIN ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *1-21* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-36,42-47 and 53* is/are rejected.

7)☐ Claim(s) *37-41 and 48-52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Sep 24, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to an amendment filed on Oct. 28, 2004, which cancels claims 1-21, and adds new claims 22-53.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 22-36, 42-47, & 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stolan (U.S. Patent number 5864663).

4. As per claims 22 & 43, Stolan teaches (col. 2, lines 46-48) a watchdog timer circuit that includes a cyclic counter counting pulses provided by a timer. As per limitations pertain to receiving refresh commands by the watchdog timer. Stolan teaches (col. 2, lines 50-52) receiving a periodic command signal from the microprocessor. As per limitations pertain to generating a microcontroller reset command by the watchdog timer when a time interval separating

successively received refresh commands is not within the predetermined range. Stolan teaches (col. 2, lines 51-53) that the failure of the microprocessor to provide this command signal causes the counter to set the over flow bit, which resets the microprocessor. He also teaches (col. 2, lines 49-51) that the counter alternately increments and decrements an output counter response to a periodic command signal from the microprocessor. He thus teaches limitations starting a refresh countdown on each receipt of a refresh command by the watchdog timer. He does not explicitly disclose to start a reset countdown if the refresh countdown has timed out, and if the refresh countdown has not timed out when a next refresh command is received, then the reset countdown is not restarted. He teaches (col. 2, lines 53-55) that the overflow bit is continuously set as the counter cycles through its maximum count as long as the microprocessor fails to provide the command signal. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that he teaches to start a reset countdown if the refresh countdown has timed out, since he teaches that the counter cycles through its maximum count as long as the microprocessor fails to provide the command signal, and furthermore, He also teaches (col. 2, lines 60-63) that the size of the counter and frequency of the timer are chosen such that the duration between reset pulses is both long enough to afford the microprocessor adequate time to prohibit the reset. Thereby clearly providing the ability to a person of ordinary skill in the art to prohibit restarting of the reset countdown.

5. As per claims 23 & 44, He also teaches (col. 2, lines 60-63) that the size of the counter and frequency of the timer are chosen such that the duration between reset pulses is both long enough to afford the microprocessor adequate time to prohibit the reset. He thus clearly provides the ability for the reset countdown to restart only if the refresh countdown has timed out,

indicating that the counter has cycled through its maximum count as long as the microprocessor fails to provide the command signal.

Double Patenting

6. Claims 24 & 45 are objected to under 37 CFR 1.75 as being a substantial duplicate of claim 23. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

7. As per claim 25, He teaches (col. 2, lines 60-64) that the size of the counter and frequency of the timer are chosen such that the duration between reset pulses is both long enough to afford the microprocessor adequate time to prohibit the reset and yet still short enough to cause the microprocessor to reset quickly after entering an aberrant state. He thus would allow the reset countdown and the refresh countdown to restart simultaneously on receipt of the next refresh command.

8. As per claims 26 & 27, He teaches (Fig. 1) clocks 40 & 42 synchronizing the reset countdown and the refresh countdown.

9. As per claims 28 & 53, He teaches (col. 4, lines 3-5) that when the user mode select signal 28 is set for the programming mode, the multiplexer disconnects the counter's overflow bit and the normal clock signal from the microprocessor and replaces them with a programming reset signal on a line 42 and a programming clock signal 44 on a line 46. He thus allows the programming duration of the reset countdown.

10. As per claim 29, He teaches (col. 3, lines 37-39) a timer 14 that provides a serial timing pulse signal on a line 16 to a counter 18. The counter 18 continually increments or decrements the current count stored in its register at the frequency of the timing pulses. He thus teaches that the refresh command for defining the duration of the reset countdown.

11. As per claim 30, He teaches as stated per claim 29 above that a timer 14 that provides a serial timing pulse signal on a line 16 to a counter 18. The counter 18 continually increments or decrements the current count stored in its register at the frequency of the timing pulses. He thus teaches that his counter defines the duration of the reset countdown based on the timing pulses.

12. As per claim 31, He teaches (col. 3, lines 37-39) a timer 14 that provides a serial timing pulse signal on a line 16 to a counter 18. The counter 18 continually increments or decrements the current count stored in its register at the frequency of the timing pulses, unless prevented by the microprocessor from reaching the upper or lower counting limit, the counter pulses its overflow bit. He thus teaches to generate a reset command by transition of the high-order bit to a low logic value.

13. As per claim 32, Stolan teaches substantially teaches the claimed invention as disclosed related to claim 22 above. As per limitations pertain to a refresh counter receiving refresh commands by the watchdog timer. Stolan teaches (col. 2, lines 50-52) receiving a periodic command signal from the microprocessor. As per limitations pertain to generating a microcontroller reset command by the watchdog timer when a time interval separating successively received refresh commands is not within the predetermined range. Stolan teaches (col. 2, lines 51-53) that the failure of the microprocessor to provide this command signal causes the counter to set the over flow bit, which resets the microprocessor. He also teaches (col. 2,

lines 49-51) that the counter alternately increments and decrements an output counter response to a periodic command signal from the microprocessor. He thus teaches limitations starting a refresh countdown on each receipt of a refresh command by the watchdog timer. He does not explicitly disclose to start a reset countdown if the refresh countdown has timed out, and if the refresh countdown has not timed out when a next refresh command is received, then the reset countdown is not restarted. He teaches (col. 2, lines 53-55) that the overflow bit is continuously set as the counter cycles through its maximum count as long as the microprocessor fails to provide the command signal. It would have been obvious to a person of ordinary skill in the art to realize that he teaches to start a reset countdown if the refresh countdown has timed out, since he teaches that the counter cycles through its maximum count as long as the microprocessor fails to provide the command signal, and furthermore, He also teaches (col. 2, lines 60-63) that the size of the counter and frequency of the timer are chosen such that the duration between reset pulses is both long enough to afford the microprocessor adequate time to prohibit the reset. Thereby clearly providing the ability to a person of ordinary skill in the art to prohibit restarting of the reset countdown.

14. As per claim 33, He also teaches (col. 2, lines 60-63) that the size of the counter and frequency of the timer are chosen such that the duration between reset pulses is both long enough to afford the microprocessor adequate time to prohibit the reset. He thus clearly provides the ability for the reset countdown to restart only if the refresh countdown has timed out, indicating that the counter has cycled through its maximum count as long as the microprocessor fails to provide the command signal.

Double Patenting

15. Claim 34 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 23. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

16. As per claims 35, 36, 46 & 47, He teaches (col. 3, lines 45-47) MSB of the word stored in the register of the counter and based on the MSB status, the microprocessor periodically instructs the counter to change its counting direction, thereby he teaches the high-order bit connected to the reset output.

Allowable Subject Matter

17. Claims 37, 38, 39-41, 48- 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. As per claim 42, He teaches (col. 4, lines 3-5) that when the user mode select signal 28 is set for the programming mode, the multiplexer disconnects the counter's overflow bit and the normal clock signal from the microprocessor and replaces them with a programming reset signal on a line 42 and a programming clock signal 44 on a line 46. He thus allows the programming duration of the reset countdown.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

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